IN THE SPECIFICATION

Please replace the paragraphs in the specification as rewritten below:

On pages 15 and 16, paragraph 51:

[0051] One objective of the present invention is to increase the speed in which the SCR 202 turns on. Recall that in the prior art, the N+ doped region 110 reduced the gain of the PNP transistor of the SCR because of the high recombination of the hole-electron pairs. Decreasing the turn on time of the SCR 202 is realized by two particular differences over the prior art. The first difference is a reduction in the size of the respective base regions of the transistors T1 231 and T2 232 in the SCR 202. The dimensions W_P and W_N in FIG. 3 represent the respective base widths of the NPN transistor T1 231 and the PNP transistor T2 232. The base widths W_N and W_P are respectively measured from the edge 311 of the P+ region 308 to the junction 307, and from the edge 313 of the N+ region 312 to the junction 307. Reducing the size (i.e., base width) of the base of each transistor T1 231 and T2 232 of the SCR 202 reduces the time it takes for the minority carriers to diffuse through these regions and reach the corresponding collector regions. The transistors T2 232 and T1 231 preferably have as small as possible (as permitted by the semi-conductor process specifications) base widths W_N and W_P. For example, the base widths W_N and W_P are less than 4.0 microns, and in one embodiment, the base widths W_N and W_P are both in a range of 0.6 to 0.8 microns.